

### Amendments to the Claims

This corrected listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:
  - a silicon-controlled rectifier (SCR) including a transistor integrally formed with the SCR, the transistor including a gate located over a channel between a first doped region of the SCR and a second doped region of the SCR;
  - a contact pad coupled to the SCR; and
  - a control circuit to change a first holding voltage of the SCR to a second holding voltage less than the power supply voltage to keep the SCR in latch-up for a time period between 150ns and 500ns in response to detecting an ESD event, and to change the second holding voltage of the SCR to ~~the first a~~ holding voltage at least to the power supply voltage after a time period to keep the SCR from latching-up, ~~wherein the control circuit is coupled only to the SCR at the second doped region.~~
2. (Currently Amended) The circuit of claim 1, wherein the control circuit includes a resistor-capacitor (RC) circuit selected to provide an RC time constant corresponding to the time period between 150ns and 500ns. ~~time period is determined by an RC constant of the control circuit.~~
3. (Previously Presented) The circuit of claim 1, the control circuit further comprising a resistor, a capacitor and an output terminal of the control circuit disposed between the resistor and the capacitor.
4. (Canceled)

5. (Original) The circuit of claim 1, the SCR further comprising a p-type substrate, an n-well and an n-well formed in the p-type substrate, a p-type diffused region formed in the n-well, and an n-type diffused region formed outside of the n-well.

6-15. (Canceled)

16. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:

a plurality of contact pads;

a plurality of silicon-controlled rectifiers (SCR), each SCR associated with one of the plurality of contact pads, each SCR including a transistor integrally formed with the SCR, wherein for each of the SCRs, a gate of the transistor is coupled to the contact pad or ground; and

a plurality of control circuits, each control circuit coupled to one of the SCRs, the control circuit to change a first holding voltage of the SCR to a second holding voltage less than the power supply voltage to keep the SCR in latch-up for a time period between 150ns and 500ns in response to detecting an ESD event, and to change the second holding voltage of the SCR to the first holding voltage at least up to the power supply voltage after a time period to keep the SCR from latching-up.

17 – 20 (Canceled)

21. (Currently Amended) The circuit of claim 16, wherein each of the control circuits includes a resistor-capacitor (RC) circuit selected to provide an RC time constant corresponding to the time period between 150ns and 500ns. ~~time period is determined by an RC constant of the control circuit.~~

22. (Previously Presented) The circuit of claim 16, wherein each control circuit comprises an output terminal coupled to a gate of a p-type and an n-type transistor associated with each SCR.

23 – 32 (Canceled)